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| QFO-AP-VA-008 | **رمز النموذج :** | **اسم النموذج : خطة المادة الدراسية** | **جامعة فيلادلفيا**  Philadelphia University |
| 2 | **رقم الإصدار: (Rev)** | **الجهة المصدرة:**  نائب الرئيس للشؤون الأكاديمية |
| 4-5-2021 | **تاريخ الإصدار:** | **الجهة المدققة :** اللجنة العليا لضمان الجودة |
| 4 | **عدد صفحات النموذج :** |

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| **Course code: 0721350** | **Course Title: Computer Organization and Architecture** |
| **Course prerequisite (s) and/or corequisite (s):**  **0750230** | **Course Level: 3 (SE BSc)** |
| **Credit hours: 3** | **Lecture Time: 15:00 – 15:50** |
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| **Academic Staff Specifics** | | | | |
| **E-mail Address** | **Office Hours** | **Office Location** | **Rank** | **Name** |
| [aobidat@philadelphia.edu.jo](mailto:aobidat@philadelphia.edu.jo) | س ن12:30-14:15  11:00 – 12:45ح ث | **331** | **Teacher** | 1. **Obidat** |

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| **The Learning Style Used in Teaching the Course** | | | |
| **Blended Learning** | | | |
| **Electronic Learning** | | | |
| **Face-to-Face Learning** | | | |
| **Percentage** | **Blended** | **Electronic** | **Face-to-Face** |
| **100%** |  |  |

**Software Engineering BSc Program**

**Course/ module description:**

The module emphasizes on the following knowledge areas: Digital components used in the organization and design of digital computer, serial and parallel transfer, Flow of information and timing signals, design an elementary basic computer, organization and architecture of the central processing unit.

**Course/ module objectives:**

**Objectives of this module are to:**

* **Introduce organization of the computer components.**
* **Introduce architecture of the computer components.**
* **Introduce organization and architecture of the central processing unit**

**Course/ module components**

* **Books (author (s), title, publisher, year of publication):**

**Computer architecture / Kin Spiner (Author).- New York: Larsen and Keller Education , 2020**

* **Support material:** Slides**.** downloaded in lecturer web page

* **Homework and laboratory guide (s) if (applicable):** downloaded in lecturer Webpage

**Teaching methods**

Duration: 16 weeks, 48 hours in total. Lectures, Tutorial, project and home works. Exams 4h.

* Face to face (30 h):
* Asynchronous (15 h):

**Learning outcomes**

A student completing this course unit should be able to:

**Knowledge and Understanding:**

*A1. Recognize a wide range of hardware used* in *organization and design of a basic digital computer.(A2)*

*A2. Identify the basic structure of central processing unit. (A3)*

**Cognitive skills (thinking and analysis):**

*B1. Discover how computer basic unit interact with each other to execute program instructions.(B1)*

*B2. Distinguish the communication (input/output) issues.(B3)*

**Practical skills:**

*C1. Identify* *the common blocks required in a typical computer system. (C2)*

**Transferable skills:**

*D1. Use creativity to Solve problems.(D3)*

**Learning Outcomes Achievements**

**A2 and C1 are achieved through lectures and assessed by quizzes and examinations**

**A1, B1, B2, C1, and D1 are achieved and assessed by homework**

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| **Allocation of Marks** | |
| **Mark** | Assessment Instruments |
| **30** | Mid Exam |
| **30** | Homework, Assignment, Forum, Glossary and quizzes |
| **40** | Final examination: 40 marks |
| **100** | Total |

**Documentation and academic honesty**

* Documentation style (with illustrative examples)

- Practical works reports must be presented according to the style specified in the homework and practical work guide

* Protection by copyright
* Avoiding plagiarism

- Any stated plagiarism leads to an academic penalty

**Course/module academic calendar**

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| **Week** | **Basic and support material to be covered** | **Learning style** |
| **(2 and 1)** | **Review of Digital Circuit and Digital Components**   * Logic Gates. * Boolean Function and Simplifications. * Combinational Circuit and Sequential circuit. * Decoders and Multiplexers. * Registers and Memory. | **Face to face: 2 h**  **Asynchronous: 1h** |
| **(4 and 3)** | **Register Transfer and Micro-operations**   * Register Transfer language and Register Transfer. * Bus and Memory Transfers. * Arithmetic Micro-operations. * Logic Micro-operations. * Shift Micro-operations.   Arithmetic Logic Shift Unit. | **Face to face: 4 h**  **Asynchronous: 2h** |
| **(5, 6 and7)** | **Basic Computer Organization and Design**   * Instruction Codes. * Computer Registers. * Computer Instructions.   - Instruction Cycle. | **Face to face: 6 h**  **Asynchronous: 3h** |
| **(9 and 8)** | **Instruction Types**   * Memory-Reference Instructions. * Register-Reference Instructions.   Input/Output Instructions.  ***Mid Term Exam:*** | **Face to face: 4 h**  **Asynchronous: 2h**  ***Mid Term Exam* face to face** |
| **(11 and 10)** | **PROGRAMMING THE BASIC COMPUTER**   * Introduction * Machine Language * Assembly Language * Program Loops   Subroutines  **Mid Exam** | **Face to face: 4 h**  **Asynchronous: 2h** |
| **(13 and 12)** | **Central Processing Unit**   * General Register Organization. * Stack Organization: Register Stack, Memory Stack. * Instruction Format: zero, one, two, and three-address instructions. * Addressing Modes.   Data Transfer and Manipulation. | **Face to face: 4 h**  **Asynchronous: 2h** |
| **(14 and 15)** | **Pipelining**   * Pipelining Definition. * The Basic Pipeline For MIPS * The Major Hurdle of Pipelining-Structural Hazards * Data Hazards * Control Hazards   Pipelining implementation | **Face to face: 4 h**  **Asynchronous: 2h** |
| 16 | **Revision and Written Final Exam** | ***Final Exam* face to face** |

**Expected workload**

On average students need to spend 2 hours of study and preparation for each 50-minute lecture/tutorial.

**Attendance policy**

Absence from lectures and/or tutorials shall not exceed 15%. Students who exceed the 15% limit without a medical or emergency excuse acceptable to and approved by the Dean of the relevant college/faculty hall not be allowed to take the final examination and shall receive a mark of zero for the course. If the excuse is approved by the Dean, the student shall be considered to have withdrawn from the course.

**Module references**

**1. Computer Organization and Architecture: designing for performance, Stallings, William, Pearson, 2016 10th edition 2016.  .**

**2. The Architecture of Computer Hardware and System Software, Irv Englander, John Wiley and Sons, 2000, 2nd edition.**

**3. Fundamentals Of Computer Organization And Architecture. Mostafa Abd-El-Barr, Hesham El-Rewini. John Wiley and Sons, 2005, 2nd edition.**

**4. Computer System Architecture, M. Morris Mano. Prentice Hall, International edition, 1998. 3rd edition.**

**Journals:**

**Article title COMPUTER ARCHITECTURE AND ORGANIZATION IN THE MODEL**

**COMPUTER ENGINEERING CURRICULUM**

**Author Nelson, V. P. Theys, M. D. Clements, A.**

**Journal title FRONTIERS IN EDUCATION CONFERENCE**

**Bibliographic details 2003, VOL 2, pages F2F-11-F2F-16**

**Publisher STIPES**

**Country of publication USA**

**Web resources**

<http://ecourse.philadelphia.edu.jo/login/index.php>.

<http://williamstallings.com/COA6e.html>

http://www.ece.eng.wayne.edu/~gchen/ece4680/lecture-notes/lecture-notes.html